L Number	Hits	Search Text	DB	Time stamp
1	2	257/797.ccls. and (alignment adj mark) and semiconductor and (stud or column) and opaque and trench and insulating and material	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 12:21
2	11	257/797.ccls. and (alignment adj mark) and semiconductor and (stud or column) and trench	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 12:21
3	1	257/797.ccls. and (alignment adj mark) and semiconductor and (stud or column) and trench and (vertical adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 12:24
4	1	257/797.ccls. and (alignment adj mark) and semiconductor and (stud or column) and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 12:24
5	1	257/797.ccls. and (alignment adj mark) and semiconductor and (stud or column or step) and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 12:24
6	0	(vertical adj gate adj transistor) and @ad<20011201 and (stud or step or column) and trench and (alignment adj mark)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 12:28
7	10	(vertical adj transistor) and @ad<20011201 and (stud or step or column) and trench and (alignment adj mark)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 12:30
8	1	(vertical adj transistor) and @ad<20011201 and (stud or column) and trench and (alignment adj mark)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 12:30
-	548	alignment adj mark and semiconductor and mask and opaque	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 13:40
-	4	alignment adj mark adj region and semiconductor and mask and opaque and trench and insulating and material	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/10 17:23
-	1	alignment adj mark adj region and semiconductor and mask and (opaque adj layer) and trench and insulating and material	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/10 17:22 ✓
-	1	alignment adj mark adj region and semiconductor and mask and opaque and trench and insulating and material and (stud or column)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/10 17:23
-	33	alignment adj mark and semiconductor and mask and opaque and trench and insulating and material	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 17:40
-	4	257/797.ccls. and alignment adj mark and semiconductor and mask and opaque and trench and insulating and material	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 12:20
-	33	alignment adj mark and semiconductor and mask and trench and insulating and material and opaque	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/12 14:47
-	250	alignment adj mark and semiconductor and mask and trench and insulating and material	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 19:13
-	1	(alignment adj mark) and semiconductor and mask and opaque and trench and (insulating or insulation) and (vertical adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 17:43

-	7	alignment adj mark and semiconductor and mask and trench and insulating and material and vertical adj transistor	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 18:28
-	7	alignment adj mark and semiconductor and mask and trench and insulating and vertical adj transistor	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 18:45
-	7	alignment adj mark and semiconductor and mask and trench and insulating and vertical adj transistor and step	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 18:50
-	1	alignment adj mark and semiconductor and mask and trench and insulating and vertical adj transistor and (step adj feature)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 18:53
-	1	alignment adj mark and semiconductor and mask and isolation adj trench and insulating and vertical adj transistor and (step adj feature)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 18:53
-	3	alignment adj mark and semiconductor and mask and isolation adj trench and insulating and vertical adj transistor	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 19:06
-	3	alignment adj mark and semiconductor and mask and isolation adj trench and insulating and vertical adj transistor and step	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 19:06
-	3	alignment adj mark and semiconductor and mask and isolation adj trench and insulating and vertical adj transistor and step	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 19:11
-	1	alignment adj mark and semiconductor and mask and isolation adj trench and insulating and vertical adj transistor and step adj feature	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 19:11
-	6	alignment adj mark and semiconductor and mask and trench and insulating and (step adj feature or design) and vertical adj transistor	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/14 19:15
-	144	alignment adj mark and semiconductor and mask and trench and insulating and (step adj feature or design)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:20
-	0	jp-1237661-$.did.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 11:46
-	0	jp-0001237661-$.did.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 11:48
-	2	jp-2000164497-$.did.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 11:57
-	2	6313542.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:01
-	2	4748103.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 11:55
-	2	jp-2000150358-$.did.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:09
-	2	5965303.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:02

-	2	5573890.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:02
-	2	5573890.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:03
-	2	5702848.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:04
-	2	5356824.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:11
-	0	ep-558401-.did.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:06
-	0	ep-0000558401-.did.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:06
-	2	4564585.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:08
-	2	20030119274.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:09
-	2	jp-2002075846-$.did.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:10
-	2	5972793.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:12
-	3	3573975.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:13
-	2	6114215.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:14
-	0	alignment adj mark and semiconductor and mask and trench and ((insulating or insulation) adj trench) and (step adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:18
-	5	alignment adj mark and semiconductor and mask and trench and insulating and (step adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 13:55
-	0	alignment adj mark and semiconductor and mask and (insulation adj trench) and (step adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:22
-	0	alignment adj mark and semiconductor and mask and (isulation adj trench) and (step adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:22
-	6	alignment adj mark and semiconductor and mask and (isolation adj trench) and (step adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 12:24
-	6	(alignment adj mark) and semiconductor and mask and (isolation adj trench) and (step adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:29

-	0	257/797.ccls. and alignment adj mark and semiconductor and mask and trench and insulating and (step adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/15 13:58
-	1	438/401,400,424,.ccls. and alignment adj mark and semiconductor and mask and trench and insulating and (step adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 10:13
-	10	438/401,400,424,404.ccls. and alignment adj mark and semiconductor and mask and opaque and trench and insulating and material	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/10/16 18:31
-	2	(alignment adj mark) and semiconductor and mask and opaque and (vertical adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:21
-	3	(alignment adj mark) and (trench adj stud) and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 13:51
-	40	(vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 13:51
-	0	(vertical adj gate adj transistor) and ad@20011201	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 13:53
-	25	(vertical adj gate adj transistor) and @ad<20011201	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 13:53
-	5	(vertical adj gate adj transistor) and @ad<20011201 and stud	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 13:54
-	3	(vertical adj gate adj transistor) and @ad<20011201 and stud and trench	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:01
-	0	(vertical adj gate adj transistor) and @ad<20011201 and stud and trench and (alignment adj mark)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 12:25
-	0	(vertical adj gate adj transistor) and @ad<20011201 and stud and trench and (mark)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:03
-	3	(vertical adj gate adj transistor) and @ad<20011201 and stud and trench and (alignment)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:12
-	0	(vertical adj gate adj transistor) and @ad<20011201 and stud and trench and (alignment adj mark)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:04
-	2	20020196651.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:28
-	1	20020196651.pn. and alignment	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:07
-	1	20020197801.pn. and alignment	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:08
-	1	6610573.pn. and alignment	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:11

-	0	6049137.pn. and (vertical adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:13
-	0	6049137.pn. and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:14
-	0	6049137.pn. and (vertical)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:14
-	1	6049137.pn. and (transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:15
-	0	6303458.pn. and (transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:16
-	1	257/797.ccls. and (alignment adj mark) and semiconductor and mask and opaque and (vertical adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:23
-	2	438/400,401,404,424.ccls. and (alignment adj mark) and semiconductor and mask and opaque and (vertical adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:24
-	3	438/400,401,404,424.ccls. and (alignment adj mark) and semiconductor and (vertical adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:28
-	2	438/400,401,404,424.ccls. and (alignment adj mark) and semiconductor and (vertical adj transistor) and stud	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:27
-	2	438/400,401,404,424.ccls. and (alignment adj mark) and semiconductor and (vertical adj transistor) and (trench adj stud)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:37
-	0	5500392.ccls. and (alignment adj mark) and semiconductor and (vertical adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:28
-	2	5500392.pn. and (alignment adj mark) and semiconductor	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:30
-	2	5500392.pn. and (alignment adj mark) and semiconductor and vertical	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:35
-	0	5500392.pn. and (alignment adj mark) and semiconductor and vertical and stud	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:35
-	0	5500392.pn. and (alignment adj mark) and semiconductor and vertical and trench	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:36
-	2	438/400,401,403,404,410,412,413,416,417,423,425,431 and (alignment adj mark) and semiconductor and (vertical adj transistor) and (trench adj stud)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 14:40
-	0	60498137.pn. and (alignment adj mark) and semiconductor and (vertical adj transistor) and (trench adj stud)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:05
-	2	5897371.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:07

-	1	5897371.pn. and trench	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:07
-	0	5897371.pn. and trench and vertical	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:07
-	1	5897371.pn. and trench and (vertical adj gate transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:09
-	1	5897371.pn. and trench and (vertical adj gate transistor) and trench	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:09
-	0	5897371.pn. and trench and (vertical adj gate transistor) and trench adj stud	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:09
-	0	5897371.pn. and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:10
-	0	6030897.pn. and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:11
-	0	6030897.pn. and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:12
-	0	6049137.pn. and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:12
-	0	6080635.pn. and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:12
-	0	6271602.pn. and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:13
-	0	5897371.pn. and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:14
-	0	6303458.pn. and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:14
-	0	2003015779.pn. and trench and (vertical adj gate adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/19 15:14
-	2	438/401,400,424,.ccls. and alignment adj mark and semiconductor and mask and trench and insulating and ((step or stud) adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 10:15
-	2	438/400,401,404,424,.ccls. and alignment adj mark and semiconductor and mask and trench and insulating and ((step or stud) adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 10:16
-	2	438/400,401,404,424.ccls. and alignment adj mark and semiconductor and mask and trench and insulating and ((step or stud) adj (feature or design))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/07/20 10:16